between a source region and a drain region. Independent claim 30 is amended herein to recite a channel comprising a silicon-germanium (Si-Ge) alloy underneath and adjacent a gate oxide. Independent claim 33 is amended herein to recite a silicon-germanium to silicon ($Si_{1-x}Ge_x/Si$) heterojunction formed between the substrate and the channel region.

Applicant respectfully submits that Nayak et al. describes a device structure having an undoped silicon cap layer between the $Ge_{0.2}Si_{0.8}$ layer and the gate oxide. Thus, Nayak et al.'s $Ge_{0.2}Si_{0.8}$ layer is not adjacent the gate oxide as the undoped silicon cap layer is interposed between these two features. Accordingly, Applicant respectfully submits that Nayak et al. does not teach nor suggest each and every feature of independent claims 11, 24, 28 and 30.

Furthermore, Applicant respectfully submits that Nayak et al. describes a device structure having an undoped silicon setback layer interposed between the $Ge_{0.2}Si_{0.8}$ layer and the n-type silicon substrate. Thus, Nayak et al.'s heterostructure does not teach nor suggest a silicon-germanium to silicon heterojunction formed between the substrate and the channel region. Accordingly, Applicant respectfully submits that Nayak et al. does not teach nor suggest each and every feature of independent claim 33.

In light of the foregoing, Applicant respectfully submits that independent claims 11, 24, 28, 30 and 33 are patentably distinct from Nayak et al. Furthermore, as claims 12-14 further define patentably distinct claim 11, claim 26 further defines patentably distinct claim 24, claim 29 further defines patentably distinct claim 28, claim 31 further defines patentably distinct claim 30 and claims 34-35 further define patentably distinct claim 33, these claims should also be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) in view of Nayak et al., and allowance of claims 11-14, 24, 26, 28-31 and 33-35.

Claims 25, 32 and 37 were rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103 as obvious over Nayak et al.

Claim 25 is amended herein to reflect independent claim format, including all elements of the intervening base claim, i.e., claim 24 prior to amendment. Applicant respectfully submits that altering claim format from dependent to independent is not made in response to any art rejection. Claim 32 is amended herein to recite *the* gate oxide rather than *a* gate oxide to reflect

proper antecedence given the amendment of claim 30. Accordingly, Applicant respectfully submits that the amendment to claim 32 is not made in response to any art rejection.

While Applicant recognizes that process limitations are not determinative of patentability in a product-by-process claim, as noted in the rejection, Applicant respectfully submits that patentability must consider the structure implied by the process. *See* MPEP § 2113.

Applicant respectfully submits that ion implanting germanium (Ge) into the substrate as provided in claim 25, ion implanting Ge ions through a gate oxide on the substrate as provided in claim 32 or ion implanting germanium (Ge) ions through a gate oxide layer on the substrate as provided in claim 37 each produce a structure inherently different from the structure described by Nayak et al. As noted previously, Nayak et al. describes a device structure having an undoped silicon cap layer between the $Ge_{0.2}Si_{0.8}$ layer and the gate oxide and an undoped silicon setback layer interposed between the $Ge_{0.2}Si_{0.8}$ layer and the n-type silicon substrate.

Applicant respectfully submits that using the process of claim 25 would preclude Nayak et al.'s undoped silicon setback layer. Applicant further respectfully submits that using the process of either claim 32 or 37 would preclude Nayak et al.'s undoped silicon cap layer. Therefore, Applicant respectfully submits that the product structures implied by the process limitations of claims 25, 32 and 37 are each patentably distinct from the structure described by Nayak et al. Furthermore, as claim 32 further defines patentably distinct claim 30, it is additionally expected to be patentably distinct on this basis alone. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102(b) and 103 in view of Nayak et al., and allowance of claims 25, 32 and 37.

Sato et al.

Claims 30 and 31 were rejected under 35 U.S.C.§ 102(b) as anticipated by Sato et al. (U.S. Patent No. 5,285,088).

As noted previously, claim 30 is amended herein to recite a channel comprising a silicon-germanium (Si-Ge) alloy underneath and adjacent a gate oxide. Applicant has carefully reviewed the Sato et al. reference and is unable to identify a feature corresponding to Applicant's gate oxide. Therefore, Applicant respectfully submits that Sato et al. does not teach nor suggest a channel comprising a silicon-germanium (Si-Ge) alloy underneath and adjacent a gate oxide,

and thus cannot anticipate claim 30. As claim 31 further defines patentably distinct claim 30, this claim should also be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b), and allowance of claims 30-31.

Claims 32 and 37 were rejected under 35 U.S.C.§ 102(b) as anticipated by or, in the alternative, under 35 U.S.C.§ 103 as obvious over Sato et al.

While Applicant recognizes that process limitations are not determinative of patentability in a product-by-process claim, as noted in the rejection, Applicant respectfully submits that patentability must consider the structure implied by the process. *See* MPEP § 2113.

Applicant respectfully submits that ion implanting Ge ions through a gate oxide on the substrate as provided in claim 32 or ion implanting germanium (Ge) ions through a gate oxide layer on the substrate as provided in claim 37 each produce a structure inherently different from the structure described by Sate et al. As noted previously, Sato et al. does not exhibit a feature corresponding to Applicant's gate oxide.

Applicant respectfully submits that using the process of claims 32 and 37 thus preclude the structures described in Sato et al. Therefore, Applicant respectfully submits that the product structures implied by the process limitations of claims 32 and 37 are each patentably distinct from the structure described by Sato et al. Furthermore, as claim 32 further defines patentably distinct claim 30, it is additionally expected to be patentably distinct on this basis alone. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102(b) and 103 in view of Sato et al., and allowance of claims 32 and 37.

Selvakumar et al.

Claims 11, 14, 24, 28 and 30 were rejected under 35 U.S.C.§ 102(b) as anticipated by Selvakumar et al. (U.S. Patent No. 5,426,069).

Applicant's invention is directed to address difficulties surrounding the extremely small base widths inherent in bipolar devices and the formation of stable gate oxide layers over $Si_{1-x}Ge_x$ transistor channels. *See* specification, p. 2, ll. 12-16 and p. 3, ll. 2-4. Applicant respectfully submits that Selvakumar et al. not only failed to address the problems overcome by Applicant, but conspicuously ignored them.

As was well understood in the art at the time of filing for the Selvakumar et al. patent, i.e., April 9, 1992, such transistor devices were well into the sub-micron dimensions. Selvakumar et al. was aware of the Nayak et al. reference cited in this action, as indicated by the references cited on the cover page of the Selvakumar et al. patent. Nayak et al. describes a 0.7μm channel device. Nayak et al., Abstract. Other references predating the Selvakumar et al. filing date additionally support the fact that typical device dimensions were sub-micron at that time. *See, e.g.*, Wolf, S., Silicon Processing for the VLSI Era, Vol. 2, p. 355, table 5.2, 1990 (showing the evolution of device structures having channel lengths of 0.4μm by 1989). Yet Selvakumar et al. describes n-channel MOSFETs having channel lengths of 7μm to 10μm, an order of magnitude larger than industry-standard devices. Selvakumar et al., col. 4, ll. 9-12. In addition, Selvakumar et al. describes a gate oxide of 100nm, i.e., 1000 Angstroms. Selvakumar et al., col. 4, l. 2. Again, this is an order of magnitude thicker than devices well understood in the art at the filing date of the Selvakumar et al. patent. *See, e.g.*, Nayak et al., Fig. 1(a); Silicon Processing, p. 355, Table 5.2.

Silicon Processing defines channel lengths to be long if they exceed 2μm, and short if less than 2μm. Silicon Processing, p. 338, § 5.5. It goes on to state that a series of effects arise in short channel devices that result in significant deviations from the values predicted by long-channel models. *Id.* Accordingly, the state of the art understood that inherent characteristics of short channel devices precluded direct application of the knowledge associated with large channel devices.

Applicant notes that one of the most fundamental and serious limitations of CMOS technology resides in the p-channel device. Specification, p. 1, ll. 15-16. Generic, one-micron processes reflect such limitations in the disparate field-effect mobilities associated with n-channel and p-channel devices within a CMOS IC. *Id.* at ll. 16-18. Applicant understood the limitations of short channel devices, and addressed those limitations, while Selvakumar et al. not only ignored, but avoided those limitations by manufacturing and testing only grossly oversized n-channel devices. Applicant thus respectfully submits that the teachings of Selvakumar et al. cannot be applied to short channel devices as they were understood in the art prior to the filing date of the Selvakumar et al. patent.

Applicant has noted that when a $Si_{1-x}Ge_x$ layer is formed on a silicon substrate, by MBE or UHV CVD, stable gate oxides can not be later formed on the $Si_{1-x}Ge_x$ layer as oxides of Ge are not stable. Specification, p. 2, ll. 18-20. Applicant respectfully submits that Selvakumar et al.'s apparent success in forming a gate oxide layer over the SiGe layer is due to the gross oversizing of the device dimensions. Given Selvakumar et al.'s failure to manufacture or test devices having channel lengths of less than 7μm in the face of industry-standard devices having dimensions an order of magnitude smaller, Applicant respectfully submits that Selvakumar et al. does not teach, suggest nor enable devices having dimensions of less than 7μm.

While Applicant respectfully submits that the devices described in Selvakumar et al. have no application to the instant claims, Applicant is willing to further clarify the differences from the instant claims and the Selvakumar et al. reference. Applicant herein amends claims 11, 24, 28 and 30 to recite channel lengths of less than 7μm. Applicant respectfully submits that this recitation more carefully clarifies the patentably distinct differences between the instant claims and Selvakumar et al. As claim 14 further defines patentably distinct claim 11, this claim should also be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) in view of Selvakumar et al., and allowance of claims 11, 14, 24, 28 and 30.

Claims 25, 32 and 37 were rejected under 35 U.S.C.§ 102(b) as anticipated by or, in the alternative, under 35 U.S.C.§ 103 as obvious over Selvakumar et al.

While Applicant recognizes that process limitations are not determinative of patentability in a product-by-process claim, as noted in the rejection, Applicant respectfully submits that patentability must consider the structure implied by the process. *See* MPEP § 2113.

Applicant respectfully submits that Selvakumar et al. does not teach nor suggest that Ge ions can be implanted through Selvakumar et al.'s 1000 Angstrom gate oxide. In addition, Applicant respectfully submits that Ge ion implanting at the energy of approximately 20 to 100 keV, as recited by the instant claims, would inherently produces a structure different from that described by Selvakumar et al. given its 1000 Angstrom gate oxide. Accordingly, ion implanting Ge ions through a gate oxide on the substrate as provided in claim 32 or ion implanting germanium (Ge) ions through a gate oxide layer on the substrate as provided in claim 37 each produce a structure inherently different from the structure described by Selvakumar et al.

Applicant respectfully submits that using the process of claims 32 and 37 thus preclude the structures described in Selvakumar et al. Therefore, Applicant respectfully submits that the product structures implied by the process limitations of claims 32 and 37 are each patentably distinct from the structure described by Selvakumar et al. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102(b) and 103 in view of Selvakumar et al., and allowance of claims 32 and 37.

Applicant herein amends claim 25 to recite a channel length of less than 7μm. As noted previously, Selvakumar et al., in their conspicuous disregard for the state of the art at the time of filing, does not teach nor suggest devices having channel lengths of less than 7μm. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102(b) and 103 in view of Selvakumar et al., and allowance of claim 25.

Crabbe' et al.

Claims 30, 31, 33 and 34 were rejected under 35 U.S.C.§ 102(e) as anticipated by Crabbe' et al. (U.S. Patent No. 5,821,577).

The Crabbe' et al. patent was issued October 13, 1998 based on a filing date of November 30, 1992. Since Crabbe' et al. issued after the effective filing date of the present application (i.e., September 18, 1996), Crabbe' et al. may be properly defined as a reference under 35 U.S.C. § 102(e). Since Crabbe' et al. may be a reference defined under 35 U.S.C. § 102(e), it is a removable reference if Applicant proves a date of invention predating November 30, 1992 (the filing date of the Crabbe' et al. patent). Applicant respectfully reserves the right to file a Petition under 37 C.F.R. § 1.131 to swear behind the Crabbe' et al. patent. However, because Applicant deems Crabbe' et al. to be distinguishable from the instant claims, Applicant at this time does not choose to remove Crabbe' et al. as a reference, but reserves exercising this right for a later date.

Similar to Nayak et al., Crabbe' et al. describes a device structure having a cap layer interposed between the SiGe channel layer and a gate insulator layer, as well as a spacer layer interposed between the SiGe channel layer and the substrate. Accordingly, and in light of the arguments presented for Nayak et al., Applicant respectfully submits that the structures recited in claims 30 and 33 are patentably distinct from the structure of Crabbe' et al. Crabbe' et al.'s SiGe

channel layer is not adjacent its gate insulator layer, and its heterochannel is not formed between its SiGe channel layer and its substrate. As claim 31 further defines patentably distinct claim 30 and claim 34 further defines patentably distinct claim 33, these claims should also be allowable. Accordingly, Applicant respectfully request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) in view of Crabbe' et al., and allowance of claims 30, 31, 33 and 34.

Claims 32 and 37 were rejected under 35 U.S.C.§ 102(e) as anticipated by or, in the alternative, under 35 U.S.C.§ 103 as obvious over Crabbe' et al.

While Applicant recognizes that process limitations are not determinative of patentability in a product-by-process claim, as noted in the rejection, Applicant respectfully submits that patentability must consider the structure implied by the process. *See* MPEP § 2113.

Applicant respectfully submits that ion implanting Ge ions through a gate oxide on the substrate as provided in claim 32 or ion implanting germanium (Ge) ions through a gate oxide layer on the substrate as provided in claim 37 each produce a structure inherently different from the structure described by Crabbe' et al. As noted previously, Crabbe' et al. describes a device structure having a cap layer interposed between the SiGe channel layer and a gate insulator layer, as well as a spacer layer interposed between the SiGe channel layer and the substrate. Therefore, Applicant respectfully submits that the product structures implied by the process limitations of claims 32 and 37 are each patentably distinct from the structure described by Crabbe' et al. Furthermore, as claim 32 further defines patentably distinct claim 30, it is additionally expected to be patentably distinct on this basis alone. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102(b) and 103 in view of Crabbe' et al., and allowance of claims 32 and 37.

Rejections Under 35 U.S.C.§ 103

Selvakumar et al. in view of Crabbe' et al.

Claims 12-13, 26, 27, 29, 31 and 33-35 were rejected under 35 U.S.C.§ 103 as being unpatentable over Selvakumar et al. together with Crabbe' et al.

Applicant respectfully submits that there is no suggestion, either express or implied, that Selvakumar et al. may be combined with Crabbe' et al. Applicant further respectfully submits that Selvakumar et al. in fact teaches away from combining the teachings of Crabbe' et al. As

noted earlier, Crabbe' et al. describes a device structure having a cap layer interposed between the SiGe channel layer and a gate insulator layer, as well as a spacer layer interposed between the SiGe channel layer and the substrate. The Crabbe' et al. structure is not obtainable by the process of Selvakumar et al. and it is, therefore, incompatible with the teachings of Selvakumar et al.

Furthermore, Selvakumar et al. does not teach nor suggest independent claims 11, 24, 28 and 30. Crabbe' et al., as a secondary reference, does not overcome the deficiencies of the primary reference. As claims 12 and 13 further define patentably distinct claim 11, claims 26 and 27 further define patentably distinct claim 24, claim 29 further defines patentably distinct claim 28 and claim 31 further defines patentably distinct claim 30, these claims should also be allowable. In addition, Selvakumar et al. does not teach nor suggest devices having channel lengths of less than 7μm. Crabbe' et al., as a secondary reference, does not overcome the deficiencies of the primary reference. Accordingly, Applicant respectfully submits that Selvakumar et al. in view of Crabbe' et al. does not teach nor suggest the transistor of independent claim 33. As claims 34 and 35 further define patentably distinct claim 33, these claims should also be allowable.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. § 103 in view of Selvakumar et al. and in further view of Crabbe' et al., and allowance of claims 12-13, 26, 27, 29, 31 and 33-35.

Maeda et al. in view of Selvakumar et al.

Claims 11, 12, 14, 24, 25, 28-30, 32-34, 36 and 37 were rejected under 35 U.S.C.§ 103 as being unpatentable over Maeda et al. (U.S. Patent 5,512,772) together with Selvakumar et al.

The Maeda et al. patent was issued April 30, 1996 based on a filing date of September 20, 1994. Since Maeda et al. issued less than one year before the effective filing date of the present application (i.e., September 18, 1996), Maeda et al. may be properly defined as a reference under 35 U.S.C. § 102(e). Since Maeda et al. may be a reference defined under 35 U.S.C. § 102(e), it is a removable reference if Applicant proves a date of invention predating September 20, 1994 (the filing date of the Maeda et al. patent). Applicant respectfully reserves the right to file a Petition under 37 C.F.R. § 1.131 to swear behind the Maeda et al. patent. However, because Applicant

deems Maeda et al. to be distinguishable from the instant claims, Applicant at this time does not choose to remove Maeda et al. as a reference, but reserves exercising this right for a later date.

Applicant respectfully submits that there is no suggestion, either express or implied, that Maeda et al. may be combined with Selvakumar et al. Applicant has noted the concerns associated with extremely small base widths inherent in bipolar devices. Specification, p. 2, ll. 12-16. This was knowledge well known at the time of filing for both the Maeda et al. and Selvakumar et al. references. Silicon Processing, p. 338, § 5.5 (noting that a series of effects arise in short channel devices that result in significant deviations from the values predicted by long-channel models). *Id.* Therefore, Applicant respectfully submits that given the conspicuous disregard of short channel devices by Selvakumar et al. in light of the state of the art at its filing date, these references may not be combined.

Applicant taught that it had not been possible to adapt $Si_{1-x}Ge_x/Si$ heterojunction technology to ICs having extremely small base widths prior to Applicant's disclosure. *See* specification, p. 2, ll. 12-16. There is no teaching nor suggestion that Selvakumar et al. may be applied to ICs having extremely small base widths. In fact, Selvakumar et al. conspicuously manufactured and tested only devices having dimensions an order of magnitude larger than the state of the art at the time of filing. Therefore, Applicant respectfully submits that it is impermissible hindsight reconstruction to combine the teachings of Selvakumar et al. with Maeda et al., as the application of Selvakumar et al. to small base width devices must rely on Applicant's own disclosure.

Applicant respectfully submits that this proposition is further supported by Maeda et al. in that Maeda et al. utilized SiGe in the construction of bipolar transistor B (*see* Maeda et al., col. 2, ll. 34-37), yet failed to incorporate what the rejection implies to be an obvious improvement, i.e., a SiGe channel, in associated transistor M2. Furthermore, Applicant respectfully submits that even if the combination is permissible, the combined references do not teach nor suggest each and every element of the instant claims. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103 in view of Maeda et al. and further in view of Selvakumar et al., and allowance of claims 11, 12, 14, 24, 25, 28-30, 32-34, 36 and 37.

Maeda et al. in view of Selvakumar et al. and Crabbe' et al.

Claims 13, 26, 27 and 31 were rejected under 35 U.S.C.§ 103 as being unpatentable over Maeda et al. together with Selvakumar et al. and Crabbe' et al.

As noted above, Applicant respectfully submits that it is impermissible to combine Selvakumar et al. with Maeda et al., in that there is no suggestion to combine the references absent Applicant's own disclosure, and that even when combined, these two references fail to teach or suggest each and every element of independent claims 11, 24 and 30. Crabbe' et al. as a secondary reference does not overcome the deficiencies of the other two references. As claim 13 further defines patentably distinct claim 11, claims 26 and 27 further define patentably distinct claim 24 and claim 31 further defines patentably distinct claim 30, these claims should also be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103 in view of Maeda et al. and further in view of Selvakumar et al. and Crabbe' et al., and allowance of claims 13, 26, 27 and 31.

CONCLUSION

Applicant believes the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. The Examiner is invited to telephone the below-signed attorney at 612-371-2103 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **March 15, 1999**.

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